

IDS - 06/10/2006



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EV669636124US

174/285

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : David Lewis et al.
Application No. : 10/766,464
Confirmation No. : 3178
Filed : January 27, 2004
For : ERROR CORRECTION FOR PROGRAMMABLE
LOGIC INTEGRATED CIRCUITS
Art Unit : 2113
Examiner : Robert W. Beausoliel, Jr.

Mail Stop AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

New York, New York 10020
March 10, 2006

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §§ 1.56 and 1.97,
applicants hereby make the following references of record
in the above-identified patent application:

U.S. Patent Documents

TB	4,005,405	West	01/25/1977
↓	4,375,664	Kim	03/01/1983
	4,866,717	Murai et al.	09/12/1989
	5,111,464	Farmwald et al.	05/05/1992
	5,305,324	Demos	04/19/1994
	5,495,491	Snowden et al.	02/27/1996
	5,511,211	Akao et al.	04/23/1996
	5,581,198	Trimberger	12/03/1996
	5,588,112	Dearth et al.	12/24/1996

U.S. Patent Documents

TB	5,754,566	Christopherson et al.	05/19/1998
	5,978,952	Hayek et al.	11/02/1999
	6,024,486	Olarig et al.	02/15/2000
	6,065,146	Bosshart	05/16/2000
	6,101,614	Gonzales et al.	08/08/2000
	6,223,309	Dixon et al.	04/24/2001
	6,279,128	Arnold et al.	08/21/2001
	6,349,390	Dell et al.	02/19/2002
	6,701,480	Karpuszkka et al.	03/02/2004
	6,832,340	Larson et al.	12/14/2004
	6,838,899	Plants	01/04/2005
	6,839,868	Pignol	01/04/2005
	6,847,554	Satori	01/25/2005
	6,848,063	Rodeheffer et al.	01/25/2005
	6,859,904	Kocol et al.	02/22/2005
	7,007,203	Gorday et al.	02/28/2006

U.S. Published Documents

TB	2004/0230767	Bland et al.	11/18/2004
	2005/0040844	Plants	02/24/2005
	2005/0044467	Leung et al.	02/24/2005
	2005/0073884	Gonzalez et al.	04/07/2005
	2005/0144551	Nahas	06/30/2005
	2005/0154943	Alexander et al.	07/14/2005

Foreign Patent Documents

TB	JP 61101857 (Abstract)	Japan	05/20/1986
	JP 62251949 (Abstract)	Japan	11/02/1987
	WO 98/29811	PCT	07/09/1998
	EP 1 100 020	EPO	05/16/2001

Non-Patent Documents

- TB Bazes et al., "Programmable NMOS DRAM Controller for Microcomputer Systems with Dual-port Memory and Error Checking and Correction," IEEE Journal of Solid-State Circuits, Vol. SC-18, No. 2, April 1983, Abstract.
- Ahrens et al., "Predictive Maintenance for Prevention of Uncorrectable Multiple BIT Errors in MEMORY," IP.com, Prior Art Database, January 28, 2005, pp. 1-5 (originally published: IBM TDB, August 1, 1989, pp. 239-244).
- Matsumoto, "Million-gate architecture will vie with ASIC-like approach from Altera, Lucent and GateField - size matters, says Xilinx with Virtex launch," Electronic Engineering Times, October 26, 1998.
- Mahmood et al., "Concurrent Error Detection Using Watchdog Processors - A Survey," IEEE Transactions on Computers, Vol. 37, No. 2, February 1998, Abstract.
- Michinishi et al., "Testing for the programming circuit of SRAM-based FPGAs," IEICE Transactions on Information and Systems, Vol. E82-D, No. 6, 1999, Abstract.
- Wang et al., "SRAM Based Re-programmable FPGA for Space Applications," IEEE Transactions on Nuclear Science, Vol. 46, No. 6, December 1999, pp. 1728-1735.
- Huang et al., "A memory coherence technique for online transient error recovery of FPGA configurations," Proceedings of the 2001 ACM/SIGDA 9th International Symposium on Field Programmable Gate Arrays, February 11-13, 2001, pp. 183-192.
- "Antifuse FPGA shoots for the stars," EDN, Vol. 48, No. 12, May 29, 2003, p. 20.
- Johnson, "Multibit error correction in a monolithic semiconductor memory," IP.com Prior Art Database, September 8, 2003, pp. 1-10.
- Tradeoffs abound in FPGA design: understanding device types and design flows is key to getting the most out of FPGAs," Electronic Design, Vol. 51, No. 27, December 4, 2003, p. S1.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary) MAR 10 2006 SHEET 1 of 4 U.S. PATENT & TRADEMARK OFFICE	Application Number	10/766,464
	Filing Date	January 27, 2004
	First Named Inventor	David Lewis
	Art Unit	2113
	Examiner Name	Robert W. Beausoliel
	Attorney Docket Number	174/285
	Confirmation Number	3178

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
TB		4,005,405	01/25/1977	West	
		4,375,664	03/01/1983	Kim	
		4,866,717	09/12/1989	Murai et al.	
		5,111,464	05/05/1992	Farmwald et al.	
		5,305,324	04/19/1994	Demos	
		5,495,491	02/27/1996	Snowden et al.	
		5,511,211	04/23/1996	Akao et al.	
		5,581,198	12/03/1996	Trimberger	
		5,588,112	12/24/1996	Dearth et al.	
		5,754,566	05/19/1998	Christopherson et al.	
		5,978,952	11/02/1999	Hayek et al.	
		6,024,486	02/15/2000	Olarig et al.	
		6,065,146	05/16/2000	Bosshart	
		6,101,614	08/08/2000	Gonzales et al.	
		6,223,309	04/24/2001	Dixon et al.	
		6,279,128	08/21/2001	Arnold et al.	
		6,349,390	02/19/2002	Dell et al.	
		6,701,480	03/02/2004	Karpuszk et al.	
		6,832,340	12/14/2004	Larson et al.	
		6,838,899	01/04/2005	Plants	
		6,839,868	01/04/2005	Pignol	
		6,847,554	01/25/2005	Satori	

Examiner Signature	/Timothy Bonura/	Date Considered	09/04/2006
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 801.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Sheet 2 of 4

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U. S. PATENT DOCUMENTS

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TB		6,848,063	01/25/2005	Rodeheffer et al.	
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↓		7,007,203	02/28/2006	Gorday et al.	

U. S. PUBLISHED DOCUMENTS

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↓		2005/0044467	02/24/2005	Leung et al.	
↓		2005/0073884	04/07/2005	Gonzalez et al.	
↓		2005/0144551	06/30/2005	Nahas	
↓		2005/0154943	07/14/2005	Alexander et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				
TB		JP 61101857 (Abstract)	05/20/1986	Hitachi Ltd.		
↓		JP 62251949 (Abstract)	11/02/1987	Mitsubishi Electric Corp.		
↓		WO 98/29811	07/09/1998	Intel Corp.		
↓		EP 1 100 020	05/16/2001	Matsushita Electric Ind. Co., Ltd.		

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Signature

/Timothy Bonura/

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Sheet 3 of 4

Application Number	10/766,464
Filing Date	January 27, 2004
First Named Inventor	David Lewis
Art Unit	2113
Examiner Name	Robert W. Beausoliel
Attorney Docket Number	174/285
Confirmation Number	3178

NON PATENT LITERATURE DOCUMENTS

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TB		Bazes et al., "Programmable NMOS DRAM Controller for Microcomputer Systems with Dual-port Memory and Error Checking and Correction," IEEE Journal of Solid-State Circuits, Vol. SC-18, No. 2, April 1983, Abstract.
		Ahrens et al., "Predictive Maintenance for Prevention of Uncorrectable Multiple BIT Errors in MEMORY," IP.com, Prior Art Database, January 28, 2005, pp. 1-5 (originally published: IBM TDB, August 1, 1989, pp. 239-244).
		Matsumoto, "Million-gate architecture will vie with ASIC-like approach from Altera, Lucent and GateField - size matters, says Xilinx with Virtex launch," Electronic Engineering Times, October 26, 1998.
		Mahmood et al., "Concurrent Error Detection Using Watchdog Processors - A Survey," IEEE Transactions on Computers, Vol. 37, No. 2, February 1998, Abstract.
		Michinishi et al., "Testing for the programming circuit of SRAM-based FPGAs," IEICE Transactions on Information and Systems, Vol. E82-D, No. 6, 1999, Abstract.
		Wang et al., "SRAM Based Re-programmable FPGA for Space Applications," IEEE Transactions on Nuclear Science, Vol. 46, No. 6, December 1999, pp. 1728-1735.
		Huang et al., "A memory coherence technique for online transient error recovery of FPGA configurations," Proceedings of the 2001 ACM/SIGDA 9 th International Symposium on Field Programmable Gate Arrays, February 11-13, 2001, pp. 183-192.
		"Antifuse FPGA shoots for the stars," EDN, Vol. 48, No. 12, May 29, 2003, p. 20.
✓		Johnson, "Multibit error correction in a monolithic semiconductor memory," IP.com Prior Art Database, September 8, 2003, pp. 1-10.

Examiner
Signature

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 4 of 4

Application Number	10/766,464
Filing Date	January 27, 2004
First Named Inventor	David Lewis
Art Unit	2113
Examiner Name	Robert W. Beausoliel
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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	
TB		"Tradeoffs abound in FPGA design: understanding device types and design flows is key to getting the most out of FPGAs," Electronic Design, Vol. 51, No. 27, December 4, 2003, p. S1.
TB		Tiwari et al., "Enhanced Reliability of Finite-State Machines in FPGA Through Efficient Fault Detection and Correction," IEEE Transactions on Reliability, Vol. 54, No. 3, September 2005, pp. 459-467.

Examiner
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : David Lewis et al.
Application No. : 10/766,464
Confirmation No. : 3178
Filed : January 27, 2004
For : ERROR CORRECTION FOR PROGRAMMABLE
LOGIC INTEGRATED CIRCUITS
Group Art Unit : 2184

New York, New York 10020
October 6, 2004

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

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U.S. PATENT DOCUMENTS

TB	4,930,098	Allen	May 29, 1990
	4,930,107	Chan et al.	May 29, 1990
	4,940,909	Mulder et al.	July 10, 1990
	5,200,920	Norman et al.	April 6, 1993
	5,237,219	Cliff	August 17, 1993
	5,291,079	Goetting	March 1, 1994
	5,321,704	Erickson et al.	June 14, 1994
	5,349,691	Harrison et al.	September 20, 1994
	5,426,379	Trimberger	June 20, 1995
	5,430,687	Hung et al.	July 4, 1995
	5,466,117	Resler et al.	November 14, 1995
	5,528,176	Kean	June 18, 1996

U.S. PATENT DOCUMENTS

TB	5,543,730	Cliff et al.	August 6, 1996
	5,552,722	Kean	September 3, 1996
	5,590,305	Terrill et al.	December 31, 1996
	5,598,424	Erickson et al.	January 28, 1997
	5,598,530	Nagae	January 28, 1997
	5,606,276	McClintock	February 25, 1997
	5,608,342	Trimberger	March 4, 1997
	5,629,949	Zook	May 13, 1997
	5,640,106	Erickson et al.	June 17, 1997
	5,650,734	Chu et al.	July 22, 1997
	5,670,897	Kean	September 23, 1997
	5,680,061	Veenstra et al	October 21, 1997
	5,691,907	Resler et al.	November 25, 1997
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	5,694,399	Jacobson et al.	December 2, 1997
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	5,844,854	Lee	December 1, 1998
	5,869,980	Chu et al.	February 9, 1999
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EP 0 838 969 A2	EPO	April 29, 1998
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The Programmable Logic Data Book 1999, Xilinx,
TB pp. 4-31 to 4-37, 6-49 to 6-57, and 7-104 to 7-113.

Application Note: FPGAS, "Correcting Single-
Event Upsets Through Virtex Partial Configuration,"
TB Xilinx, XAPP216 (v1.0), June 1, 2000, pp. 1-12.

Application Note: Virtex Series, "Virtex FPGA
TB Series Configuration and Readback," Xilinx, XAPP138
(v2.7), July 11, 2002, pp. 1-39.


**U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE**
**INFORMATION DISCLOSURE
STATEMENT BY APPLICANTS**
ATTY. DOCKET NO.
174/285

APPLICATION NO.
10/766,464

APPLICANTS
David Lewis et al.

CONFIRMATION NO.
3178

FILING DATE
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GROUP
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
TB	4,930,098	05/29/90	Allen	364	716	
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	5,291,079	03/01/94	Goetting	307	465	
	5,321,704	06/14/94	Erickson et al.	371	37.1	
	5,349,691	09/20/94	Harrison et al.	395	800	
	5,426,379	06/20/95	Trimberger	326	39	
	5,430,687	07/04/95	Hung et al.	365	230.08	
	5,466,117	11/14/95	Resler et al.	414	799	
	5,528,176	06/18/96	Kean	326	105	
	5,543,730	08/06/96	Cliff et al.	326	38	
	5,552,722	09/03/96	Kean	326	41	
	5,590,305	12/31/96	Terrill et al.	395	430	
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	5,598,530	01/28/97	Nagae	395	182.19	
	5,606,276	02/25/97	McClintock	327	263	
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EXAMINER

/Timothy Bonura/

DATE CONSIDERED

09/04/2006

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FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANTS	ATTY. DOCKET NO. 174/285	APPLICATION NO. 10/766,464
	APPLICANTS David Lewis et al.	CONFIRMATION NO. 3178
	FILING DATE January 27, 2004	GROUP 2184

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
TB	5,696,454	12/09/97	Trimberger	326	38	
	5,742,531	04/21/98	Freidin et al.	364	716.03	
	5,767,734	06/16/98	Vest et al.	327	536	
	5,773,993	06/30/98	Trimberger	326	38	
	5,798,656	08/25/98	Kean	326	39	
	5,821,772	10/13/98	Ong et al.	326	38	
	5,838,167	11/17/98	Erickson et al.	326	38	
	5,844,829	12/01/98	Freidin et al.	364	716.03	
	5,844,854	12/01/98	Lee	361	230.01	
	5,869,980	02/09/99	Chu et al.	326	38	
	5,873,113	02/16/99	Rezvani	711	103	
	5,949,987	09/07/99	Curd et al.	395	500.17	
	5,961,576	10/05/99	Freidin et al.	708	232	
	5,995,744	11/30/99	Guccione	395	500.44	
	5,995,988	11/30/99	Freidin et al.	708	232	
	5,999,014	12/07/99	Jacobson et al.	326	38	
	6,011,406	01/04/00	Veenstra	326	38	
	6,018,250	01/25/00	Chiang et al.	326	38	
	6,023,565	02/08/00	Lawman et al.	395	500.02	
	6,028,445	02/22/00	Lawman	326	38	
	6,044,025	03/28/00	Lawman	365	191	
	6,049,222	04/11/00	Lawman	326	38	
	6,052,755	04/18/00	Terrill et al.	711	103	
	6,057,704	05/02/00	New et al.	326	38	
	6,069,489	05/30/00	Iwanczuk et al.	326	40	
	6,097,210	08/01/00	Iwanczuk et al.	326	39	
	6,105,105	08/15/00	Trimberger	711	103	

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANTS**

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
TB	6,128,215	10/03/00	Lee	365	154	
	6,137,307	10/24/00	Iwanczuk et al.	326	38	
	6,154,048	11/28/00	Iwanczuk et al.	326	38	
	6,184,705 B1	02/06/01	Cliff et al.	326	38	
	6,191,614 B1	02/20/01	Schultz et al.	326	41	
	6,201,406 B1	03/13/01	Iwanczuk et al.	326	38	
	6,204,687 B1	03/20/01	Schultz et al.	326	40	
	6,216,259 B1	04/10/01	Guccione et al.	716	17	
	6,237,124 B1	05/22/01	Plants	714	763	
	6,242,941 B1	06/05/01	Vest et al.	326	26	
	6,314,550 B1	11/06/01	Wang et al.	716	17	
↓	6,429,682 B1	08/06/02	Schultz et al.	326	41	
	6,560,743 B2	05/06/03	Plants	714	763	

U.S. PATENT APPLICATION

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
TB	2003/0097628 A1	05/22/03	Ngo et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
TB	EP 0 291 167 A2	11/17/88	EPO	G11B	20/18		
	EP 0 838 969 A2	04/29/98	EPO	H04Q	11/04		
↓	EP 1 100 020 A1	05/16/01	EPO	G06F	12/16		

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

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